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B: Amendments to The Claims:

What is claimed is:

1 1. (Currently Amended) A computer program on a media
2 usable with a computer for testing combinational and
3 sequential logic circuits where memory units are coupled
4 together to form shift register latches that are arranged in
5 a shift register scan path with an input and output for
6 testing the logic circuits, said computer program
7 comprising:

8 load pattern computer code for shifting data through
9 the scan path to load the shift register latches with a
10 first data pattern representative of a stuck-at fault
11 condition and thus introducing said data into an
12 inaccessible latch in a stuck-at fault LSSD chain;

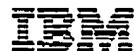
13 pattern variation computer code for causing permutation
14 of at least one of the following operating parameters: a
15 supply voltage, a reference voltage, a timing pattern
16 temperature and a timing sequence to trigger a change in
17 state of at least one of the memory units in the shift
18 register scan path for the purpose of locating stuck-at
19 fault bits in said LSSD chain; and

20 analyzing computer code for determining the memory unit
21 furthest from the shift register scan path output that has
22 changed state from its loaded value for the purpose of
23 locating stuck-at fault bits in said at least one of the
24 memory units.

1 2. (original) The computer program of claim 1, wherein said
2 pattern variation computer code is for causing permutations
3 in a plurality of the operating parameters.

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2 3. (original) The computer program of claim 2, wherein said
3 analyzing computer code includes shifting code for shifting
4 data out of the scan path after each of the operating
parameters is separately permuted.

1

2 4. (Previously Amended) The computer program of claim 3,
3 wherein said analyzing computer code includes selection
4 computer code for selecting the last bit read out that has
5 changed from its load pattern as being from the shift
register latch closest to the stuck-at fault condition.

1

2 5. (currently amended) A method for testing combinational
3 and sequential logic circuits where memory units are coupled
4 together to form shift register latches, arranged in a shift
5 register scan path with an input and output for testing the
6 logic circuits, the method comprising:

7 determining a stuck-at fault condition exists in one of
8 the shift register latches;

9 shifting data through the scan path to load the shift
10 register latches with a first data pattern representative of
11 the outputs state as a result of the stuck-at fault
12 condition and thus introducing said data into an
13 inaccessible latch in a stuck-at fault LSSD chain;

14 causing permutation of at least one of the following
15 operating parameters: a supply voltage; a reference
16 voltage; a timing pattern temperature and a timing sequence
17 to trigger a change in state from the stuck-at fault state
18 of at least one of the memory units in the shift register
19 scan path for the purpose of locating stuck-at fault bits in
20 said stuck-at fault LSSD chain; and

21 determining the memory unit furthest from the shift
22 register scan path output that has changed state from its
23

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loaded value for the purpose of locating stuck-at fault bits
1 in said at least one of the memory units.

2

3 6. (Previously Amended) The method of claim 5 including:
4 causing permutations in a plurality of the operating
parameters in determining said memory unit furthest from the
1 shift register scan path output.

2

3 7. (original) The method of claim 6 including:
4 shifting data out of the scan path after each of the
1 operating parameters is separately permuted.

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3 8. (Previously Amended) The method of claim 7 including:
4 selecting the last bit read out that has changed from
its load pattern as being from the shift register latch
1 closest to the stuck-at fault memory condition.

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3 9. (Previously submitted) The method of claim 5 including
loading all shift register latches of the scan chain with
1 stuck fault output state.

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3 10. (Currently Amended) A computer program on a media usable
4 with a computer for testing combinational and sequential
5 logic circuits where memory units are coupled together to
6 form shift register latches that are arranged in a shift
7 register scan path with an input and output for testing the
8 logic circuits, said computer program comprising:

9 stuck fault detection code for detecting a stuck-at
10 fault output level of the shift register scan path from an
11 expect state;

12 load pattern computer code for shifting data through
13 the scan path to load the shift register latches of the scan
14 path with the detected stuck-at fault output level condition

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15 and thus introducing said data into an inaccessible latch in
16 a stuck-at fault LSSD chain;

17 pattern variation computer code for causing permutation
18 of at least one of the following operating parameters: a
19 supply voltage, a reference voltage, a timing pattern
20 temperature and a timing sequence to trigger a change in
21 state of at least one of the memory units in the shift
22 register scan path that is detectable at the output of the
23 shift register scan path for the purpose of locating
24 stuck-at fault bits in said stuck-at fault LSSD chain; and
25 analyzing computer code for determining the memory unit
26 furthest from the shift register scan path output that has
27 changed state from its loaded value as a result of
28 permutations of an operating parameter for the purpose of
1 locating stuck-at fault bits in said at least one of the
 memory units.

2

3 11. (Previously submitted) A computer program of claim 10
1 including masking code for masking out all expects for
 latches following and including a farthest failing latch.

2

3 12. (Previously submitted) The computer program of claim
4 11, wherein said pattern variation computer code is for
5 causing permutations in a plurality of the operating
6 parameters centered around a working threshold varying the
1 operating parameters in the vicinity of the working
 threshold.

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3 13. (Previously submitted) The computer program of claim 12,
4 wherein said analyzing computer code includes shifting code
 for shifting data out of the scan path after each of the
1 operating parameters is separately permuted.

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3 14. (Currently Amended) The computer program of claim 11,
4 wherein said analyzing computer code includes selection
5 computer code for selecting the last bit read out that has
6 changed from its load pattern as being from the shift
register latch closest to ~~the a stuck-at fault~~ memory unit
having a stuck-at fault.

C: Remarks:

The undersigned talked with the Examiner the week of April 1, 2005 and having received the rejection then discussed thanks the Examiner for his careful examination and suggestion as to the claims which have been adopted. The suggestion that language relating to "introducing said data into an inaccessible latch in a stuck-at fault LSSD chain"..and then to trigger a change in state of at least one of the memory units in the shift register scan path that is detectable at the output of the shift register scan path for the purpose of locating stuck-at fault bits in said stuck-at fault LSSD chain has been introduced into each independent claim. This is acknowledged as not shown in the art.

Any further changes in language that the examiner believe appropriate can be agreed to by telephone if required and this amendment suggested by the examiner is being faxed to make sure early consideration results in a statement of allowable subject matter.